TDI TEST VERIFICATION MATRIX

REQUIREMENT	DESCRIPTION	TEST PLAN SECTION	TEST VERIFICATION METHOD	TEST CASE NUMBER
TDI-GEN-00010	Data streaming into TDI shall be supported as combined QPSK and redundant data streams for ULDB missions		I	
TDI-GEN-00020	The TDI shall not interleave the I and Q channels and it shall support the LDB missions as independent I and Q channel data flow s		I	
TDI-GEN-00030	Each flight computer shall have a dedicated TDI board that exists w ithin the PC-104 flight computer stack.			
TDI-GEN-00040	The TDI shall use the low er 8 bits (SD0-SD7) of the PCI 104 16-bit bus for all IO operations.		A	
TDI-ADR-00105	Data entering the TDI shall use an 8-bit asynchronous parallel data bus.		A	
TDI-ADR-00110	The TDI shall use SA9-SA2 of the PCI-104 address bus to determine TDI base I/O address selection. A minimum of 16 bytes shall be used to segment the base I/O.		A	
TDI-ADR-00115	In the ULDB mission configuration, read and w rite functions to a single address shall execute independently on both streams simultaneously. In the LDB mission configuration, read and w rite functions are independently addressed for each data stream.	3.1	D	Reg Test
TDI-ADR-00120	ULDB missions shall use a single clock rate configuration register address for both I and Q data rates. LDB missions shall use tw o clock rate configuration register addresses for independent clock rate settings.	3.1,3.2	D	Reg Test ClkRate Test
TDI-CLK-00105	The TDI shall generate its ow n 2X clock for convolutional encoding. The clock shall be programmable via the flight computer's 8-bit data bus.	3.2	D	ClkRate Test
TDI-CLK-00110	The TDI shall support at a minimum the follow ing agile data clock frequency range on each of the I and Q data stream: 1KHZ to 150Khz w ith 0.1% accuracy. Note any clock frequency should be achieved by replacing the crystal oscillator on the TDI board.	3.2	T	ClkRate Test
TDI-CLK-00115	The data clock frequency settings in the clock register shall not be affected by a soft reset from the flight computer.	3.4,4.1	D	Reset Test SFT
TDI-CLK-00120	There shall be tw o separate clock rate configurations for reading data from each FIFO in support of independent I and Q data rates for the LDB missions.	3.1,3.2,3.5,3.6,3.7,4.1	D	Reg Test ClkRate Test Bert Test Unenc Test Conv Test SFT

TDI TEST VERIFICATION MATRIX

REQUIREMENT	DESCRIPTION	TEST PLAN SECTION	TEST VERIFICATION METHOD	TEST CASE NUMBER
TDI-CLK-00125	An 8-bit clock register shall be used to configure the 2X clock frequency. This register shall server as one of the write functions and occupy 1 byte of I/O	3.1	D	Reg Test
TDI-DAT-00105	The RSTDRV line from the PC-104 flight computer bus shall be used for all TDI hard resets.	3.4	T	Reset Test
TDI-DAT-00110	A hard reset from the flight computer shall cause all FIFO and encoder shift register data to be cleared while placing the write and read FIFO pointers to the bottom or beginning of the FIFO	3.4,4.1	D	Reset Test SFT
TDI-DAT-00115	A hard reset from the flight computer shall set the configuration register to raw data, encoded at rate 1/2	3.4,4.1	D	Reset Test SFT
TDI-DAT-00120	The TDI shall support a soft reset by the flight computer by enabling a reset TDI write function. A software reset to the FIFO(s) shall cause all FIFO data to be cleared and move the Read and Write pointers to the bottom or beginning of the FIFO(s).	3.4,4.1	D	Reset Test SFT
TDI-DAT-00125	A hard reset from the flight computer shall disable the clock and set the configuration register to 0.	3.4,4.1	D	Reset Test SFT
TDI-DAT-00130	The clock shall remain disabled after a hard reset until a frequency setting other than 0 is placed in the clock register by the flight computer.	3.4,4.1	D	Reset Test SFT
TDI-DAT-00205	FIFO status monitors shall be at a minimum the Empty Flag(EF), the Half Full flag (HF) and Full Flag for each FIFO.	3.3	D	FIFO Test
TDI-DAT-00210	The HF flag on each FIFO shall drive a selectable interrupt request (IRQ) line on the flight computer. This IRQ line shall be used to request the flight computer to write data into the TDI FIFO(s).	3.3	D	FIFO Test
TDI-DAT-00305	Each read/write function shall occupy one 8-bit address byte.	3.1	D	Reg Test
TDI-DAT-00310	An 8-bit configuration register shall control the configuration of each TDI data stream.	3.1,3.5,3.6,3.7,4.1	D	Reg Test Bert Test Unenc Test Conv Test SFT
TDI-DAT-00315	The three LSB PC-104 address lines, SA0-SA2 shall be used to decode all read and write functions.	3.1	D	Reg Test

TDI TEST VERIFICATION MATRIX

REQUIREMENT	DESCRIPTION	TEST PLAN SECTION	TEST VERIFICATION METHOD	TEST CASE NUMBER
TDI-DAT-00320	At a minimum the configuration register shall enable/disable encoded data, raw data, and a BERT pattern of 2**11-1 pseudo random data (PRN). Placement of these functions in the configuration register is left to the designer.	3.5,3.6,3.7,4.1	D	Bert Test Unenc Test Conv Test SFT
TDI-DAT-00325	The contents of the configuration register shall not be affected by a soft reset from the flight computer.	3.4,4.1	D	Reset Test SFT
TDI-DAT-03105	There shall be at a minimum the following read functions on the TDI: read FIFO status, read clock register and read configuration register. Address designations for each read function are left to the designer.	3.1,3.3	D	Reg Test FIFO Test
TDI-DAT-03110	All read functions on the TDI shall use the I/O read strobe line to synchronize reading of the data to from the TDI to the flight computer.	3.1	T	Reg Test
TDI-DAT-03205	There shall be at a minimum the following write functions on the TDI: TDI write, FIFO data write, clock register write, and configuration register write. Placement of these functions in the configuration register is left to the designer.	3.1,3.3	D	Reg Test FIFO Test
TDI-DAT-03210	All TDI data and function writes shall use the I/O write strobe line from the PCI 104 bus to drive data into the TDI from the flight computer.	3.1	T	Reg Test
TDI-DAT-03215	A single FIFO write shall place data into both FIFOs for the ULDB missions. LDB missions must use independent FIFO writes to support independent data streaming into each FIFO.	3.3,3.6,3.7,4.1	D	FIFO Test Unenc Test Conv Test SFT
TDI-DAT-00405	The TDI shall convolutionally encode two data streams independently at a rate of 1/2 and constraint length 7.	3.7,4.1	D	Conv Test SFT
TDI-DAT-00410	Data shall be convolutionally encoded serially using an NRZ-L data stream.	3.7,4.1	D	Conv Test SFT
TDI-DAT-00413	An NRZ-M test point shall be provided on the TDI.	3.5,3.6,3.7,4.1	D	Bert Test Unenc Test Conv Test SFT
TDI-DAT-00415	Convolutionally encoded data shall be enabled or disabled by witting to the write configure register.	3.7,4.1	D	Conv Test SFT
TDI-DAT-00505	A BERT pattern using 2**11-1 pseudo random (PRN) code shall be generated on the TDI for data flow verification test procedures.	3.5,3.7,4.1	D	Bert Test Conv Test SFT
TDI-DAT-00510	The BERT mode shall be enabled/disabled by writing to the configuration register.	3.5,3.7,4.1	D	Bert Test Conv Test SFT

TDI TEST VERIFICATION MATRIX

REQUIREMENT	DESCRIPTION	TEST PLAN SECTION	TEST VERIFICATION METHOD	TEST CASE NUMBER
TDI-DAT-00515	While operating in the BERT mode, the flight computer shall have the continued ability to write data to the FIFOs, but the TDI shall be inhibited from reading data from the FIFOs	3.5,4.1	D	Bert Test SFT
TDI-HDW-00010	A hardware jumper shall place the TDI into a ULDB or LDB TDI mission configuration setting. The jumper shall be enabled for LDB missions and disabled for ULDB missions.	1.3	D	
TDI-HDW-00020	An 8-bit base I/O address switch must be used to allow configuration of the TDI within a given PC platform.	1.3	D	
TDI-HDW-00030	An open collector output from a PSL discrete deck shall drive a commandable selectable line for data stream selection for ULDB missions.	3.3,3.6,3.7,4.1	D	FIFO Test Unenc Test Conv Test SFT
TDI-INT-00210	Each ULDB TDI card shall output combined serial I and Q data to each TDRSS transponder telemetry channel bus input.	3.5,3.6,3.7,4.1	D	Bert Test Unenc Test Conv Test SFT
TDI-INT-00220	The TDI shall output each data stream such that it is RS422 voltage level compliant with no stop, start or parity bits. These output must conform to the EIA RS422A electrical standard.	4.2	T	IVF Test
TDI-E&M-00105	The TDI must conform to a PC-104 form factor footprint and be a stackable card that becomes part of the vertical PC-104 architecture in the ULDB flight computer	4.2	D	IVF Test
TDI-E&M-00205	The TDI shall have an operating temperature range of -30C to +50C with 0%to 95% relative humidity.	4.3	D	Thermal Test
TDI-E&M-00210	The TDI storage range shall be -55C to +85C.		A	
TDI-E&M-00215	The TDI shall follow the thermal test procedures outlined for flight qualification by the project.		D	Thermal & thermal-vacuum test
TDI-PWR-00005	The TDI shall be powered by the +5V PC-104 TTL vertical bus,	4.2	D	IVF Test
TDI-PWR-00010	No more than 5W shall be consumed by the TDI.	4.2	T	IVF Test

TDI TEST VERIFICATION MATRIX

REQUIREMENT	DESCRIPTION	TEST PLAN SECTION	TEST VERIFICATION METHOD	TEST CASE NUMBER	COMMENTS
TDI-GEN-00010	Data streaming into TDI shall be supported as combined QPSK and redundant data streams for ULDB missions		I		General statement w ill be verified by a combination of tests.
TDI-GEN-00020	The TDI shall not interleave the I and Q channels and it shall support the LDB missions as independent I and Q channel data flow s		I		General statement w ill be verified by a combination of tests.
TDI-GEN-00030	Each flight computer shall have a dedicated TDI board that exists w ithin the PC-104 flight computer stack.				General information - not a testable requirement.
TDI-GEN-00040	The TDI shall use the low er 8 bits (SD0-SD7) of the PCI 104 16-bit bus for all IO operations.		A		Verified by design analysis.
TDI-ADR-00105	Data entering the TDI shall use an 8-bit asynchronous parallel data bus.		A		Verified by design analysis.
TDI-ADR-00110	The TDI shall use SA9-SA2 of the PCI-104 address bus to determine TDI base I/O address selection. A minimum of 16 bytes shall be used to segment the base I/O.		A		Verified by design analysis
TDI-ADR-00115	In the ULDB mission configuration, read and w rite functions to a single address shall execute independently on both streams simultaneously. In the LDB mission configuration, read and w rite functions are independently addressed for each data stream.	3.1	D	Reg Test	Specific test exercised for boa #1 only. Capability inferred fro SFT on follow on boards.
TDI-ADR-00120	ULDB missions shall use a single clock rate configuration register address for both I and Q data rates. LDB missions shall use tw o clock rate configuration register addresses for independent clock rate settings.	3.1,3.2	D	Reg Test ClkRate Test	Specific test exercised for boa #1 only. Capability inferred fro SFT on follow on boards.
TDI-CLK-00105	The TDI shall generate its ow n 2X clock for convolutional encoding. The clock shall be programmable via the flight computer's 8-bit data bus.	3.2	D	ClkRate Test	Specific test exercised for boa #1 only. Capability inferred fro SFT on follow on boards.
TDI-CLK-00110	The TDI shall support at a minimum the follow ing agile data clock frequency range on each of the I and Q data stream: 1KHZ to 150Khz w ith 0.1% accuracy. Note any clock frequency should be achieved by replacing the crystal oscillator on the TDI board.	3.2	T	ClkRate Test	Specific test to exercise each the clock frequencies for boar # 1 only. Only 1Khz and 150Mh w ill be tested for accuracy to .1% A minimum of 3 clock frequencies w ill be tested by SFT on follow on boards.
TDI-CLK-00115	The data clock frequency settings in the clock register shall not be affected by a soft reset from the flight computer.	3.4,4.1	D	Reset Test SFT	
TDI-CLK-00120	There shall be tw o separate clock rate configurations for reading data from each FIFO in support of independent I and Q data rates for the LDB missions.	3.1,3.2,3.5,3.6,3.7,4.1	D	Reg Test ClkRate Test Bert Test Unenc Test Conv Test SFT	

TDI TEST VERIFICATION MATRIX

REQUIREMENT	DESCRIPTION	TEST PLAN SECTION	TEST VERIFICATION METHOD	TEST CASE NUMBER	COMMENTS
TDI-CLK-00125	An 8-bit clock register shall be used to configure the 2X clock frequency. This register shall server as one of the write functions and occupy 1 byte of I/O	3.1	D	Reg Test	Specific test exercised for boa #1 only. Capability inferred fro SFT on follow on boards.
TDI-DAT-00105	The RSTDRV line from the PC-104 flight computer bus shall be used for all TDI hard resets.	3.4	T	Reset Test	Specific test exercised to instrument HW for board #1 on Capability inferred from SFT on follow on boards.
TDI-DAT-00110	A hard reset from the flight computer shall cause all FIFO and encoder shift register data to be cleared while placing the write and read FIFO pointers to the bottom or beginning of the FIFO	3.4,4.1	D	Reset Test SFT	
TDI-DAT-00115	A hard reset from the flight computer shall set the configuration register to raw data, encoded at rate 1/2	3.4,4.1	D	Reset Test SFT	
TDI-DAT-00120	The TDI shall support a soft reset by the flight computer by enabling a reset TDI write function. A software reset to the FIFO(s) shall cause all FIFO data to be cleared and move the Read and Write pointers to the bottom or beginning of the FIFO(s).	3.4,4.1	D	Reset Test SFT	
TDI-DAT-00125	A hard reset from the flight computer shall disable the clock and set the configuration register to 0.	3.4,4.1	D	Reset Test SFT	
TDI-DAT-00130	The clock shall remain disabled after a hard reset until a frequency setting other than 0 is placed in the clock register by the flight computer.	3.4,4.1	D	Reset Test SFT	
TDI-DAT-00205	FIFO status monitors shall be at a minimum the Empty Flag(EF), the Half Full flag (HF) and Full Flag for each FIFO.	3.3	D	FIFO Test	Specific test exercised for boa #1 only. Capability inferred fro SFT on follow on boards.
TDI-DAT-00210	The HF flag on each FIFO shall drive a selectable interrupt request (IRQ) line on the flight computer. This IRQ line shall be used to request the flight computer to write data into the TDI FIFO(s).	3.3	D	FIFO Test	Specific test exercised for boa #1 only. Capability inferred fro SFT on follow on boards.
TDI-DAT-00305	Each read/write function shall occupy one 8-bit address byte.	3.1	D	Reg Test	Specific test exercised for boa #1 only. Capability inferred fro SFT on follow on boards.
TDI-DAT-00310	An 8-bit configuration register shall control the configuration of each TDI data stream.	3.1,3.5,3.6,3.7,4.1	D	Reg Test Bert Test Unenc Test Conv Test SFT	
TDI-DAT-00315	The three LSB PC-104 address lines, SA0-SA2 shall be used to decode all read and write functions.	3.1	D	Reg Test	Specific test exercised for boa #1 only. Capability inferred fro SFT on follow on boards.

TDI TEST VERIFICATION MATRIX

REQUIREMENT	DESCRIPTION	TEST PLAN SECTION	TEST VERIFICATION METHOD	TEST CASE NUMBER	COMMENTS
TDI-DAT-00320	At a minimum the configuration register shall enable/disable encoded data, raw data, and a BERT pattern of 2**11-1 pseudo random data (PRN). Placement of these functions in the configuration register is left to the designer.	3.5,3.6,3.7,4.1	D	Bert Test Unenc Test Conv Test SFT	
TDI-DAT-00325	The contents of the configuration register shall not be affected by a soft reset from the flight computer.	3.4,4.1	D	Reset Test SFT	
TDI-DAT-03105	There shall be at a minimum the following read functions on the TDI: read FIFO status, read clock register and read configuration register. Address designations for each read function are left to the designer.	3.1,3.3	D	Reg Test FIFO Test	Specific test exercised for boa #1 only. Capability inferred fro SFT on follow on boards.
TDI-DAT-03110	All read functions on the TDI shall use the I/O read strobe line to synchronize reading of the data to from the TDI to the flight computer.	3.1	T	Reg Test	Specific test exercised for boa #1 only. Capability inferred fro SFT on follow on boards.
TDI-DAT-03205	There shall be at a minimum the following write functions on the TDI: TDI write, FIFO data write, clock register write, and configuration register write. Placement of these functions in the configuration register is left to the designer.	3.1,3.3	D	Reg Test FIFO Test	Specific test exercised for boa #1 only. Capability inferred fro SFT on follow on boards.
TDI-DAT-03210	All TDI data and function writes shall use the I/O write strobe line from the PCI 104 bus to drive data into the TDI from the flight computer.	3.1	T	Reg Test	Specific test exercised for boa #1 only. Capability inferred fro SFT on follow on boards.
TDI-DAT-03215	A single FIFO write shall place data into both FIFOs for the ULDB missions. LDB missions must use independent FIFO writes to support independent data streaming into each FIFO.	3.3,3.6,3.7,4.1	D	FIFO Test Unenc Test Conv Test SFT	
TDI-DAT-00405	The TDI shall convolutionally encode two data streams independently at a rate of 1/2 and constraint length 7.	3.7,4.1	D	Conv Test SFT	
TDI-DAT-00410	Data shall be convolutionally encoded serially using an NRZ-L data stream.	3.7,4.1	D	Conv Test SFT	
TDI-DAT-00413	An NRZ-M test point shall be provided on the TDI.	3.5,3.6,3.7,4.1	D	Bert Test Unenc Test Conv Test SFT	
TDI-DAT-00415	Convolutionally encoded data shall be enabled or disabled by witting to the write configure register.	3.7,4.1	D	Conv Test SFT	
TDI-DAT-00505	A BERT pattern using 2**11-1 pseudo random (PRN) code shall be generated on the TDI for data flow verification test procedures.	3.5,3.7,4.1	D	Bert Test Conv Test SFT	
TDI-DAT-00510	The BERT mode shall be enabled/disabled by writing to the configuration register.	3.5,3.7,4.1	D	Bert Test Conv Test SFT	

TDI TEST VERIFICATION MATRIX

REQUIREMENT	DESCRIPTION	TEST PLAN SECTION	TEST VERIFICATION METHOD	TEST CASE NUMBER	COMMENTS
TDI-DAT-00515	While operating in the BERT mode, the flight computer shall have the continued ability to w rite data to the FIFOs, but the TDI shall be inhibited from reading data from the FIFOs	3.5,4.1	D	Bert Test SFT	
TDI-HDW-00010	A hardw are jumper shall place the TDI into a ULDB or LDB TDI mission configuration setting. The jumper shall be enabled for LDB missions and disabled for ULDB missions.	1.3	D		Will be implicitly tested since se of tests w ill be run in ULDB and LDB modes.
TDI-HDW-00020	An 8-bit base I/O address sw itch must be used to allow configuration of the TDI w ithin a given PC platform.	1.3	D		Will be tested implicitly since w can set different I/O base addresses for ULDB and LDB tests.
TDI-HDW-00030	An open collector output from a PSL discrete deck shall drive a commandable selectable line for data stream selection for ULDB missions.	3.3,3.6,3.7,4.1	D	FIFO Test Unenc Test Conv Test SFT	
TDI-INT-00210	Each ULDB TDI card shall output combined serial I and Q data to each TDRSS transponder telemetry channel bus input.	3.5,3.6,3.7,4.1	D	Bert Test Unenc Test Conv Test SFT	
TDI-INT-00220	The TDI shall output each data stream such that it is RS422 voltage level compliant w ith no stop, start or parity bits. These output must conform to the EIA RS422A electrical standard.	4.2	T	IVF Test	Will measure for each board
TDI-E&M-00105	The TDI must conform to a PC-104 form factor footprint and be a stackable card that becomes part of the vertical PC-104 architecture in the ULDB flight computer	4.2	D	IVF Test	Will place each board in dev system stack.
TDI-E&M-00205	The TDI shall have an operating temperature range of -30C to +50C w ith 0%to 95% relative humidity.	4.3	D	Thermal Test	"-40degC - +80degC (prototype -10degC to +70degC (flight). 3 cycles each mode. SFT executed at each plateau. Assumes use of ULDB project provided "flight like" system.
TDI-E&M-00210	The TDI storage range shall be -55C to +85C.		A		Design Analysis/Parts analysis
TDI-E&M-00215	The TDI shall follow the thermal test procedures outlined for flight qualification by the project.		D	Thermal & thermal-vacuum test	6 Thermal cycles on the Bench and a single thermal vacuum chamber cycle test at WFF
TDI-PWR-00005	The TDI shall be pow ered by the +5V PC-104 TTL vertical bus,	4.2	D	IVF Test	Demonstrate by placement in d machine stack.
TDI-PWR-00010	No more than 5W shall be consumed by the TDI.	4.2	T	IVF Test	Will measure for each board